REMARKS

This response amends claim 12 in responding to the Examiner's rejection under 35 USC 112, second paragraph. New claims 36-49 are added. Support for the new claims can be found, e.g., in Figs. 21-23 and the corresponding description. The Applicants respectfully submit that no new matter is entered.

Upon amendment, this application will have 2 independent claims (claims 1 and 36) and 28 total claims (claims 1-14 and 36-49). At the time this application was filed, official fee was paid for up to 3 independent claims and 35 total claims. Thus, no additional fee for excess claims is due.

At page 2 of the Office Action, the Examiner objects to the drawings on the basis that reference sign 36 is not included. The Applicants have amended the drawings to add reference sign 36. It is believed that this objection has been overcome.

At the end of page 2, the Examiner indicates that "DSD" should be "ESD" on page 16, line 12. The Applicants agree and have amended the specification accordingly.

At page 3 of the Office Action, the Examiner rejects claim 12 under 35 USC 112, second paragraph, suggesting that there is insufficient antecedent basis for the limitation "at the at least one first island breakdown-enhanced layer" in claim 12. Such limitation has been amended to "near the at least

one first island", which is supported by claim 1. The Applicants believe that this rejection has been overcome.

Rejections under 35 USC 103(a)

At pages 3-4 of the Office Action, the Examiner rejects claims 1, 3, 5, 7-9 and 13-14 in section 2 under 35 USC 103(a) as being anticipated by Hsue et al. (US Patent No. 5,559,352) in view of Hokazono et al. (US 2003/0141551 A1). Moreover, at page 5, claim 2 is rejected under 35 USC 103(a) as being unpatentable over Hsue et al. in view of Hokazono et al., and further in view of Ker et al. (US 2002/0076876 A1); claim 4 is rejected under 35 USC 103(a) as being unpatentable over Hsue et al. in view of Hokazono et al., and further in view of Chuang et al. (US Patent No. 6,008,080); at page 6, claim 6 is rejected under 35 USC 103(a) as being unpatentable over Hsue et al. in view of Hokazono et al., and further in view of Kuo (US Patent No. 6,268,256); at page 7, claims 10-12 are rejected under 35 USC 103(a) as being unpatentable over Hsue et al. in view of Hokazono et al., and further in view of Hsu (US Patent No. 6,100,141). These rejections are respectfully traversed.

Hsue et al., Hokazono et al., Ker et al., Chuang et al., Kuo and Hsu, standing alone or in combination, fail to disclose, teach, or suggest, *inter alia*, the following features recited by claim 1 of the present application:

"at least one first island, formed on the first drain/source region...";

and

"a doped drain region of a first-type conductivity in the first drain/source region, defined substantially by a field oxide region, the channel

region and the at least one first island".

Hsue et al. discloses an ESD protection device with reduced breakdown voltage, simultaneously with an integrated circuit which includes FET devices. However, Hsue et al. does not teach a first island formed on the first drain/source region as recited by claim 1 of the present application.

At page 3 of the Office Action, the Examiner identifies gate 20 of Hsue et al. as the first island formed on the drain/source region. The Applicants respectfully disagree. At col. 2, lines 43~48, Hsue et al. teaches that "Referring now to FIG. 1, there is shown an ESD protection device 10 and an internal FET device 12. Both devices are formed at the same time on a single P- substrate 14. Field oxide regions 16 are formed in a conventional manner, for example, by the LOCOS (LOCal Oxidation of Silicon) technique, and serve to isolate devices from one another."

Moreover, at col. 2, lines 54~56, Hsue et al. teaches that "[T]he gate layer is then patterned by conventional lithography and etching, to form a gate electrode for each device consisting of gate oxide 18 and gate 20".

According to the teaching of Hsue et al., the ESD protection device 10 and the internal FET device 12 are formed within two active regions isolated form each other by the field oxide regions 16. The two elements 20 in FIG. 7 are the gate electrodes respectively of the ESD protection device 10 and the internal FET device 12. Those skilled in the art will appreciate that two channel regions are formed respectively under the two gate electrodes 20. That is to say, in FIG. 7, Hsue et al. teaches two, not one single, active

regions, each of which is separated into two drain/source regions 32 by one of the channel regions formed under the gate electrodes 20. The elements 20 are the gate electrodes formed above the channel region rather than islands formed on the drain/source regions 32. There is no island formed on the drain/source regions 32 in FIG. 7. Thus, Hsue et al. does not teach a first island formed on the first drain/source region as recited by claim 1 of the present application.

At page 4 of the Office Action, the Examiner identifies the source/drain region 28 of Hsue et al. as the doped drain region of a first-type conductivity and the field oxide regions 16 as the at least one first island. The Applicants respectfully disagree. As previously stated, Hsue does not teach, disclose or suggest at least one first island formed on the first drain/source region. In FIG. 7, the doped drain region 32 is defined only by the field oxide regions 16 and the channel region formed under the gate electrode 20. There is no island in the doped region 32.

Hokazono et al. teaches a gate electrode provided via a gate insulating film formed between the source and drain regions. The Examiner does not show that Hokazono et al. teaches a first island, formed on the first drain/source region or a doped drain region of a first-type conductivity in the first drain/source region, defined substantially by a field oxide region, the channel region and the at least one first island, as recited by claim 1 of the present application.

Ker et al., Chuang et al., Kuo and Hsu are cited only with respect to features of the dependent claims. The Examiner does not show that the

above-quoted features of claim 1 are taught or suggested by these references.

Under MPEP 2143, to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Since the cited references do not teach or suggest the above-quoted features of claim 1, the Applicants believe that claim 1 is patentable. Claims 2-14 are also patentable, at least by virtue of their dependency from claim 1.

New claim 36 recites, in part, "at least one distributed junctions formed within the first drain/source region and completely surrounded by the first doped region; the at least one distributed junctions including a first junction being spaced apart from the channel region; and a breakdown-enhanced layer formed at an edge of the first junction." The Applicants believe that the prior art does not teach all these limitations. Thus, claim 36 is also patentable. Claims 37-49 are patentable, at least by virtue of their dependency from claim 36.

The Applicants believe that all pending claims are patentable and reconsideration of this application is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the

number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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Troy Guangyu Cai
(Name of Person Signing)

(Signature)

12/31/2003
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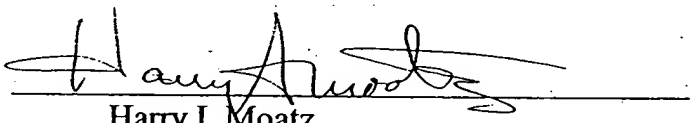

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